Progress Towards the Realization of MMIC Technology at Submillimeter Wavelengths:
A Frequency Multiplier to 320 GHz.

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ABSTRACT

The authors report on the design, analysis and performance of an all GaAs MMIC multiplier for use at submillimeter wavelengths. A novel method for coupling power in and out of the MMIC chip via a broad band photoetched ridge-waveguide-to-microstrip transition has been developed and used for this implementation. Measurements on the first iteration chipset, which implements a Schottky varactor diode doubler to 320 GHz, show a conversion efficiency of 2.8% at an input power level of 15mW. This performance is shown to be extremely well predicted by commercially available circuit simulators: HP MDS and Ansoft Maxwell. A second iteration chipset, based upon the excellent agreement between the numeric simulator and measurements on the existing circuit, is nearly complete and is expected to yield even better performance.

I. INTRODUCTION

Multipliers using GaAs MMIC technology have recently been realized at frequencies near 100 GHz using either CPW probes [1], E-plane waveguide probes [2] or ridges [3] to couple the signal into and out of the MMIC chip. The numerous advantages of MMIC technology: circuit and device flexibility, reproducibility, reliability, make this a very desirable circuit implementation for space borne radiometer applications. Towards this end, we report on what we believe is the first true GaAs MMIC multiplier circuit operating at submillimeter wavelengths. Utilizing commercially available numeric analysis codes (HP MDS and Ansoft Maxwell) with customized device models, a new photofabricated ridge-waveguide-to-microstrip (or CPW) transition design and state-of-the-art device processing, we have designed, fabricated and tested MMIC multipliers with output power at 320 and 640 GHz.

The 320 GHz doubler has a flange-to-flange efficiency of 2.8% with 15mW input power in a non-optimum circuit realization. Detailed numeric analysis of the device and circuit show excellent agreement with measured performance. A second design iteration, nearly completed, and based on the simulation results is expected to yield improved RF performance.

II. SUBMILLIMETER MMIC CHIP DESIGN

The MMIC circuit is implemented in a straight forward manner with traditional microstrip circuit elements on 50 micron thick GaAs. With this topology, radiation losses and circuit element resonances begin to pose a serious problem as the frequency exceeds about 300 GHz. At this frequency CPW elements or ultrathin membrane design realizations [1,4 for example] must be invoked. Device implementation at 300 GHz is aided by the use of air bridge Schottky diodes using rectangular (rather than circular) anodes for reduced series resistance. The diode fabrication utilizes low parasitic rectangular anode geometry and is described in [5]. For synthesis/analysis of the combined device/circuit we first developed a very accurate model of the submillimeter-wave diode junction including current saturation effects and implemented it in the HP nonlinear circuit simulator - MDS. Coupling the device model with a careful finite element simulation of the air bridge structure (using Ansoft Maxwell), made possible an optimization of the diode physical parameters (doping and junction geometry) as a function of the multiplier input/output power and frequency [6]. Measurement of a diode fabricated according to the process described in [5] shows very good agreement with a computation using our model (Fig. 1).

Given reasonable agreement between the circuit simulations and measurements at the device level, the

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diode embedding impedances required for optimum multiplier performance can now be synthesized using standard microstrip element models and realized on the MMIC chip (Fig. 2). The chip also includes the required frequency separating filters and bias circuitry. As a first iteration, the 320 multiplier design discussed in this paper utilized a non-optimum epilayer doping, and the circuits were designed using standard microstrip models from MDS, which were later found to be very inaccurate at our frequency of interest with the 50 micron thick substrate.

III. MOUNT IMPLEMENTATION

In order to couple power into and out of the MMIC chip and at the same time allow rapid insertion and removal of the device under test, we designed and implemented a ridge-waveguide-to microstrip (or CPW) transition based upon a concept described in [7]. In this realization however, the ridges are chemically milled from BeCu sheet in a photolithographic process which can be used to mass produce individual designs. The ridges are then permanently soldered into their respective positions in the E-plane of a split waveguide block (Fig. 3). Once in place, the block halves are permanently mated to form inline input and output waveguides for the multiplier. The MMIC chip is positioned on a mobile post set between the two waveguides and brought into contact with the ridge transitions via a rotating cam mechanism. The chip is held in position by pressure alone and can be quickly removed and replaced without damage to the circuit. Bias contacts are made to the chip by wire bonds from either side and can be implemented after the chip has been pinned into its final location in the block. For more permanent mounting the chip would be glued in position. The ridge coupling circuit and mount is very flexible and can also be used for mixers, detectors etc. with equal or non-equal waveguide input-output cross section and is described more fully in [8].

For the 160-to-320 GHz doubler implementation the ridges were formed from 3 and 1.5 mil thick BeCu respectively. Measurements in test blocks with 50 ohm microstrip line between the ridge transitions yields 0.5 dB insertion loss per ridge over 25% bandwidth (better than -15 dB return loss) at 160 GHz, and about 1 dB insertion loss over 20% bandwidth at 320 GHz. A photograph showing the ridges contacting the 160-320 GHz MMIC doubler chip in its waveguide block appears as Fig. 4.

IV. MEASUREMENTS AND ANALYSIS

RF measurements of multiplier performance are readily accomplished with the inline waveguide input/output ports. A swept backward wave oscillator (120-170 GHz) with 15mW maximum output power was used as a pump source and power at 320 GHz was measured with an overmoded Anritsu thermister power head calibrated against a waveguide calorimeter and a Keating acousto-optic bolometer. Measurements of the first run of 320 GHz doubler chips has provided a maximum efficiency of 2.8% over a narrow bandwidth (Fig. 5). Input coupling to the diode through the 160 GHz ridge was excellent as manifested by the resulting current flow in the device even at large reverse bias. The theoretical maximum conversion efficiency of the diode (30%), is greatly reduced however, by RF losses in the circuit at 300 GHz where radiation effects are large (non TEM modes generated in the circuit which do not couple to the output ridge). In addition the MDS circuit models for the filter and matching elements are not accurate at the output frequency of the multiplier due to the convenient-to-handle but electrically thick 50 micron GaAs substrate.

In order to accurately analyze the entire circuit and get a better understanding of the apparent losses, it was necessary to use a full three dimensional finite element analysis (HFSS/Maxwell) to determine the S parameters of each functional element. It is important with HFSS to perform the simulation on the entire structure, including the incident waveguides, ridges and microstrip circuit, to ensure that the modes are correct. Using a method which consists of replacing the active junction by a port by means of a "coaxial probe" [9], we computed the S parameters of the full passive waveguide multiplier structure. These are then inserted into MDS, and together with the diode nonlinear model, allowed an accurate computation of the expected doubler performance as a function of frequency. The result of the analysis, and comparison with measurement is given in Fig. 5. As can be seen, the agreement is very good, and shows that the circuit works as designed - although obviously not as well as we had hoped when the initial design was laid out!

The excellent agreement between the measured and predicted multiplier performance have allowed us to redesign the doubler chip layout with some confidence as to the realization of improved

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efficiency and bandwidth (20% efficiency over 10% bandwidth). We have also begun development of CPW designs for 320 and 640 GHz using modified ridge transitions.

V. ACKNOWLEDGMENTS

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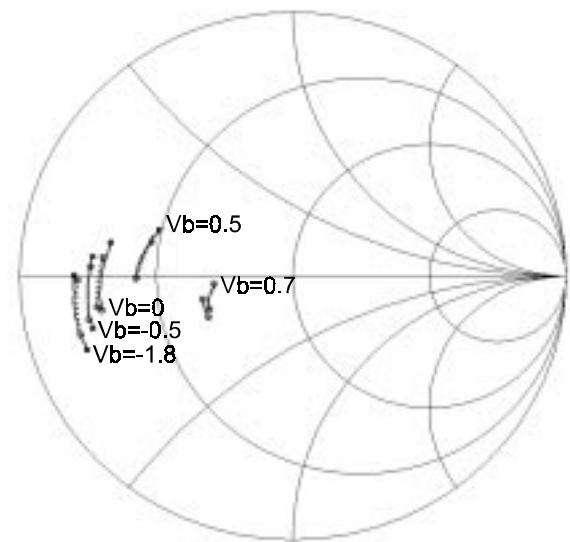
VII. FIGURES

Fig. 1. S parameters of a 1x4.6 microns square Schottky diode with an epilayer doping of $3x10^{23} m^{-3}$, embedded in its CPW test structure: Measured (continuous line) and simulated (dashed line) from 95 to 105 GHz, at different bias voltage levels Vb. The agreement is excellent and shows the accuracy of the diode model and of the simulation.
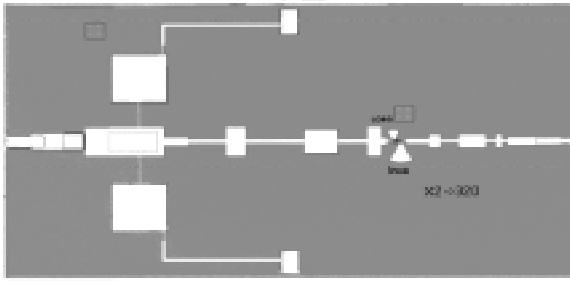
Fig. 2. Photograph of the 320 GHz MMIC doubler chip (826 x 1820 microns square), fabricated at the JPL MicroDevices Lab.
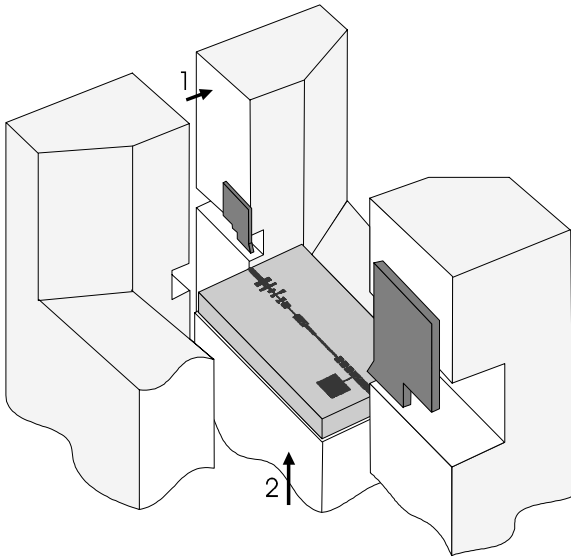

Fig. 3. Drawing of the waveguide block used for testing the MMIC chips at submillimeter wavelengths. The ridges are soldered in the E plane of the waveguide, and the two halves of the block are then permanently mated (1). The chip is then placed on top of a mobile post, which is moved upward to contact the ridges (2).
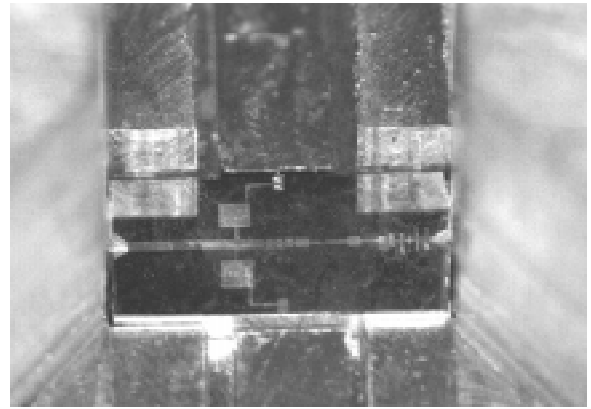

Fig. 4. Photograph of a multiplier chip mounted in the RF waveguide test block. The two ridge tips can be seen protruding on the left and right where they contact the microstrip conducting line at the center of the MMIC chip. The bias pads can be seen near the middle of the chip, to either side of the main microstrip line. The diode is towards the right side of center. The chip is riding on a moving post which pushes the ridges up against the top of the chip to make electrical contact with the microstrip line. One side of the line is DC isolated from the ridge contact by a bypass capacitor to allow DC biasing.
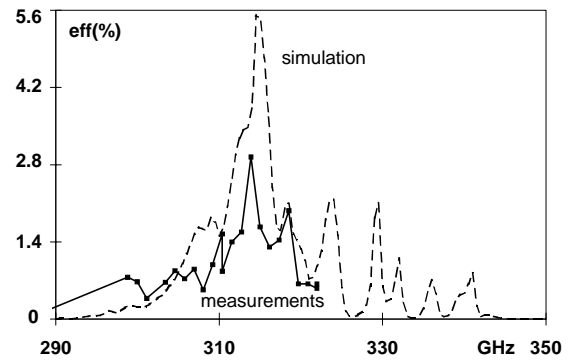

Fig. 5. Measured and computed performance of the 320 GHz MMIC doubler, showing very good agreement over frequency.

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